

Accelerating High-Speed Digital Design Workflow with Keysight ADS

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- Keysight Advanced Design System Software High Speed Digital Solutions
- ADS Memory Design Workflow Memory Designer
- ADS SerDes Design Workflow System Designer for PCIe®
- Conclusion

High Speed Digital Designs Are Already Complex!

The challenge of today's hardware designer

- Design margins continue to shrink and speed increases, there is less room for error in your design
- Hard to collate results, gather insights into the design and optimize the design
- After a small production run, it can be difficult to troubleshoot issues found
- Uncertainty for product reliability leads to significant risk to design schedules
- Hours of setup time before the first simulation
- Topology and configuration changes require multiple schematics and many parameter values to sweep through



ADS HSD Design Flow

ADS accelerate High-Speed Digital Workflows



Memory Design Workflow



What Matters in Memory Simulations?



What Are Typical Methods Used for Modeling the Channels?



SIPro Electromagnetic PCB Extraction

Layout to results in less than 20 clicks

- No layout simplification required!
- Net-driven
- Guided port creation
- Quickly plot all crosstalk elements from the same component
- Easily plot TDR/TDT
- Mixed-mode S-parameters
- One-click schematic generation



How SIPro Performs (Fast & Accurate) Analysis?





What Matters in Memory Simulations?



IBIS: Input/output Buffer Information Specification



- IBIS is an industry-standard model for characterizing inputs and outputs of Integrated Circuits
- Supplied in a data file written in text format (.ibs)
- Only the operation of the IO buffer is described
- Primary use for designing chip-to-chip serial links like Memory Modules and Boards.
- In digital circuits, from the viewpoint that it is good to consider the effects of reflection and crosstalk, a solution is sought based on the characteristic impedance of the IO buffer and wiring (reflection analysis method)
- IBIS Open Forum
 - http://www.eda-stds.org/ibis/
- IBIS 5.0 was approved in August 2008, and an Algorithmic Modeling Interface (AMI) was added to the existing specification

IBIS model

Example



• Pullup, Pulldown, Protection Diode Power Clamp, Ground Clamp, Die Capacitance (C_comp) and Package RLC



Overview of IBIS-AMI Models

Algorithmic Modeling Interface (AMI)



- Modeling interface for Memory/SerDes behavioural Models such as Equalization and Clock Data Recovery (CDR)
- Added alongside with traditional IBIS flow in IBIS version 5.0
- Acts as a Digital Signal Processing block takes input signal waveform and outputs a modified waveform
- Developed by SerDes vendors to match and represent the actual chip behaviour



Memory Interface IBIS-AMI Model Builder

DDR5/LPDDR5 and PAM-n IBIS-AMI Model building wizard

Key Takeaway Keysight ADS provided quick an easy generation of IBIS-AMI models to kick-start your simulation

ry Interface AMI Model Builder te a new AMI Model Folder or edit an existing (x one.	Don't have A You can bui	AMI model for DDR5/LPDD Id your own AMI models e
e a new AM Memory Interface AMI	Model Builder	X Memory Interface AMI Model Builder	💹 Memory Interface AMI Model Builder X
of model fo	Define ANII Parameters for RX Controller Define model parameter values or use default values. Delay Vref Calibration CTLE AGC Compression DF Prable CTLE Image: CTLE Image: Pole-zero individual values Pole-zero preset Step response	Define AMI Parameters for Rx Controller Define model parameter values or use default values. Delay Vref Calibration CTLE AGC Compression DFE Clocking Delay DFE DFE DFE_tap:	Define AMI Parameters for RX Controller Define model parameter values or use default values. Vref Calibration CTLE AGC Compression DFE Imaginary CDR: This is a DQS/CK model Use crossing times as dock Use crossing times as dock Explain forwarded dock waveform (GatVarian)
rd based IBIS Constrained File Pic 2 R R Pic 2 R R Constrained Constrained State Constrained Constrained	-AMI model building	Drocess Tap 2 -0.01 3 -0.005 4 -0.02	PI_number_phase_section: 4 PI_number_phase_step: 32 PI_parasitic_outoff_freq: Format Value Format Corner Format List Papily delay to forwarded dock Delay unit: in seconds in uI Delay unit: in seconds in uI Delay depends on signal index Delay Delay depends on agenalized Delay 2 4e-12 Ae-12
B Frequency GHz	CHE TO Format Increment typ: min: max:	Add Delete Selectr	Add Delete Selected

< Back

Next >

Save

Build

< Back

5? No problem! sily and quickly!

Extensive standard model features:

.ami

.ibs

.dll or .so

.conf (re-usable)

- Delay
- **Vref Calibration**
- CTLE
- AGC
- Compression
- DFE

٠ ...

Forward clocking (GetWave2) •

Buil

Save

< Back

KEYSIGHT

Next >



PathWave ADS Memory Designer

- Simulation Environment designed with the Memory Design Engineer in mind
- Smart bus, components, and Memory Eye Probe
- Multiple Simulation Engines
 - Transient Convolution
 - DDR BUS Sim
 - Bit-by-Bit Simulation
 - Statistical Simulation
- Compliance Report Generation
- Single-Ended PAM-4 simulation capability
- IBIS-AMI model generation wizard
- CA Data Bus Designer
- DDR extraction wizard in SIPro

and much more...





Example – Byte1 (DQ0~DQ7,DQS0 and DM0) on Platform Board

Simulation Structure, Setup, and Results



dustry prov	en measu	rement so	cience	,e 1	or sign-	511			
DR4 Test DDR4 Device 1									
View Tools Help Up Select Tests Configure Conn	ect Run Automate Resu	lts							
Test Name VSEH(Clock Plus)	Actual Value M	largin % Pass Limits Information Only	# Trials 4						
VIH.CA(AC)	764.681000000 mV 9	.2 VALUE >= VrefCA_	Volt+0.1 V 68						
tIS(base)	460.5 ps 6	42.7 VALUE >= 62.0 ps	68						
			KEYS TECHNO		DDR4 Te	est Rep	ort		
					P	ass -			
rial Summary — Actu	al Value Margin Num	OfMeas Min			Test Config	guration Det	tails		
Completed: 68 Mean 798.2 m	/ 14.03 % 8.98	35 798.2 mV	Custom Data Rate []	MT/s1 2400	Device	e Description			
assed: 68 Studey 9.027 n	V 1.373 % 1.37	0 54.93 mV	Test Mode	Custo	n				
Alled: 0 Min 764.7 n	v 9.240 % 6.00	00 764.7 mV	Burst Triggering M LPDDR4	No No	Wrt ONLY				
orst: 18 Max 819.6 n	/ 17.09 % 11.0	00 819.6 mV	LPDDR4X	No					
Sum 54.28 V	953.8% 611	.0 54.28 V			Test Se	ession Details			
Inal 18 764.68	JUUUUU MV 9.2% /	764.6809816361	Run Mode Tofiniium SW Versi	ADS A	utomation				
			Infiniium Model Nu	mber N8900	A				
			Infiniium Serial N	umber No Se	rial				
			Debug Mode Used	No No	2040.0				
			Compliance Limits	DDR4-	2400 Test Limit (official)				
<		ـــــــــــــــــــــــــــــــــــــ	ibis type	4.0	orsim (~) 510.gdevelop				
			bit_rate_gbps	2.4					
sages			Last Test Date	2019-	01-10 12:07:16 UTC -08:00				
mmaries (click for details) 019-01-24 11:49:58:408 AM Ready 019-01-24 11:49:59:025 AM Conco	d Mode Enabled	De Al	Summary o	of Resul	ts				
2019-01-24 11:50:04:463 AM Autom	tion Started		Test Statistics	s Margi	n Thresholds				
019-01-24 11:50:04:582 AM Autom	tion Ended		Failed 0	Warning	< 5 %				
019-01-24 11:50:04:691 AM Pup S	arted	F	Total 18	Chuca					
	ded								
19-01-24 11:50:04:091 AM Run o	aca	· · · · · · · · · · · · · · · · · · ·	Page # Engled	# Trials 1	est Name (click to jump)	Actual Value	Margin	Pass Limits	1
19-01-24 11:57:54:608 AM Run ei			rass # railed		ese mane (essen co Jamp)		<u> </u>	TOSS CANACS	
)19-01-24 11:57:54:608 AM Run ei			0 0	4 5	SEH(Clock Plus)	930.91600000 mV	100.0	Information Only	
019-01-24 11:57:54:608 AM Run ei				4 5 8 0 4	SEH(Clock Plus) vershoot amplitude (Address, Control) (K(abc) Rising Edge Mersurgments	930.91600000 mV -120.844700000 mV 828 ns	100.0 301.4	Information Only VALUE <= 60.00000000 mV Information Only	





Compliance_Probe Compliance_Probe

Automatically invoked and controlled by ADS

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
	0	4	VSEH(Clock Plus)	930.916000000 mV	100.0	Information Only
0	0	8	Overshoot amplitude (Address, Control)	-120.844700000 mV	301.4	VALUE <= 60.0000000 mV
	0	4	tCK(abs) Rising Edge Measurements	828 ps	100.0	Information Only
0	0	4	tjit(CC) Rising Edge Measurements	8 ps	90.4	VALUE <= 83 ps
0	0	4	tCK(avg) Rising Edge Measurements	833 ps	0.0	833 ps <= VALUE <= 937 ps
0	0	4	tjit(per) Rising Edge Measurements	8 ps	40.5	-42 ps <= VALUE <= 42 ps
0	0	4	terr(2per) Rising Edge Measurements	-7 ps	44.3	-61 ps <= VALUE <= 61 ps
0	0	4	terr(3per) Rising Edge Measurements	-6 ps	45.9	-73 ps <= VALUE <= 73 ps
0	0	4	terr(4per) Rising Edge Measurements	-6 ps	46.3	-81 ps <= VALUE <= 81 ps
0	0	4	terr(Sper) Rising Edge Measurements	-7 ps	46.0	-87 ps <= VALUE <= 87 ps
\bigcirc	0	4	terr(6per) Rising Edge Measurements	-7 ps	46.2	-92 ps <= VALUE <= 92 ps
0	0	4	terr(7per) Rising Edge Measurements	5 ps	47.4	-97 ps <= VALUE <= 97 ps
0	0	4	terr(8per) Rising Edge Measurements	-5 ps	47.5	-101 ps <= VALUE <= 101 ps
0	0	4	terr(9per) Rising Edge Measurements	5 ps	47.6	-104 ps <= VALUE <= 104 ps
0	0	4	terr(10per) Rising Edge Measurements	-5 ps	47.7	-107 ps <= VALUE <= 107 ps

Design Exploration with HTML Report

Pass/Fail & Eye, Waveform, Bathtub plots

- **Design Exploration** in Memory_Probe now supports HTML report
- Pass/Fail for scalar measurements, otherwise output only plots (eye density, waveform data, bathtub, etc)
- Requires "Datalink" installation

KEYSIGHT						
		Memory Desig	iner Repoi	t		
		Configuration	n Details			
		Design Name D	DesignExploration_DC	R		
		Simulation Mode	DDRSim			
		Dram Type	DDR4			
		Data Rate	1600 Mbps			
		Data Cycle	Write			
		Data Cycle Mode	Continuous			
		Number of Batch Points	3			
		Summary of Sc	alar Results			
		Ch0_U1_RxO	utput_A0			
	Measurement	Value	Deviation(%)	Range	Pass or Fail	
	Eye Height	0.78 V	420	0.15 V to inf V	Pass	
	Eye Width	1:19375e-09 sec (0.955 UI)	98.9583	6.00000e-10 sec to inf sec (0.48 UI to inf UI)	Pass	
	SlewRate Rise Min	4.71644	34.5993	0.4 to 7	Pass	
	SlewRate Rise Max	4.79631	33.3892	0.4 to 7	Pass	
	SlewRate Fall Min	4.56749	36.8562	0.4 to 7	Pass	
	SlewRate Fall Max	4.73761	34.2787	0.4 to 7	Pass	
	Height At BER = 1e-16	1.197 V	698	0.15 V to inf V	Pass	
	Width At BER = 1e-16	1.197 V	698	0.15 V to inf V	Pass	
	Mask Margin Timing Margin UL	4.02610e-10 sec (0.322088 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass	
	Mask Margin Timing Margin UR	3.97390e-10 sec (0.317912 UI)	NA	u sec to inf sec (0 UI to inf UI)	Pass	
	Mask Margin Timing Margin LL	3.90110e-10 sec (0.312088 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass	
	Mask Margin Timing Margin LR	4.03640e-10 sec (0.322912 UI)	NA	0 sec to inf sec (0 UI to inf UI)	Pass	
	Mask Margin Voltage Margin UL	0.33975 V	NA	0 V to inf V	Pass	
	Mask Margin Voltage Margin UR	0.50175 V	NA	0 V to inf V	Pass	
	Mask Margin Voltage Margin LL	0.40125 V	NA	0 V to inf V	Pass	
	Mask Margin Voltage Margin LR Skew Min	0.53825 V 2.89763e-10 sec (0.231811	NA	0 V to inf V NA	Pass	
	Skew Mean	UI) 2.96778e-10 sec (0.237422 UI)	NA	NA	NA	
	Skew May	3.04433e-10 sec (0.243546	NA	NA	NA	







Summary of Supported Memory Interfaces

Best design platform for Memory Systems



One Tool, Multiple Standards Covered!

SerDes Design Workflow



SerDes Design Workflow

High-Speed Channel Simulation enables Chip-to-Chip Link Analysis

- ADS's Channel simulation enables complete chip-tochip link analysis
- IBIS-AMI Modeling supported (PCIE5 AMI Modeler, USB4 AMI Modeler, etc)
- Verify high speed digital signal and power integrity design for standards like PCI Express®, Ethernet, DDR, HDMI, USB and SATA.



Key Takeaway Keysight ADS covers multiple SerDes applications

What Matters in PCIe Simulations?

Simulator, Chipset Models, Channel models





Root Complex

- Interface between CPU, Memory and the rest of PCIe Interface

Retimer

- ee at high data rata
- Compensate loss at high data rate
 Recovers timing of bits received
- and retransmits the bit sequence

Endpoint

- PCIe End Component/Devices (E.g SSD, GPU)



What Matters in PCIe Simulations?

Simulator, Chipset Models, Channel models

RC to Retimer/Retimer to Endpoint Channel



System Designer for PCIe[®]

A smarter design workflow for PCIe applications



- Streamlined design and simulation workflow for PCIe applications, Gen5 and Gen6 (PAM4) •
 - Supports multi-links and multi-lanes PCIe system .
 - PCIe_RootComplex, PCIe_EndPoint, PCIe_Repeater, PCIe_Simulator, PCIe_PreLayout, PCIe_PostLayout, PCIe_Tline, • PCIe Probe, PCIe Compliance Probe, and PCIe Setup



Supports Seasim Interface ۰

- Included PCIe Compliance Tests •
- Included PCIe AMI model builder •



Example – Byte1 (DQ0~DQ7,DQS0 and DM0) on Platform Board



Investigate Pro-Comp	liance for Sign_Off	
investigate Fre-Comp	mance for Sign-On	PCIe Probe
DDR4 Test DDR4 Device 1 File View Tools Help Set Up Select Tests Configure Connect Run Automate Results Test Name Actual Value Margin % Pass Limits VSEH(Clock Plus) 842.762500000 mV Information Only VIHLCA(C) 764.88000000 mV 9.2 VALUE >= VrefCA Vierschedt amplitude (Address Conterf) -523.38000000 mV 9.2 VALUE >= 0.000	cience # Trials 4 Volt+0.1 V 68 D00000 mV fee	
ttS(base) 460.5 ps 642.7 VALUE >= 62.0 ps	68	PCIe_Probe PCIe_Probe
Trial Summary Actual Value Margin NumOfMeas Min Completed: 68 Mean 798.2 mV 14.03 % 8.985 798.2 mV Fassed: 68 StdDev 9.627 mV 1.375 % 1.377 9.627 mV Failed: 0 Range 54.92 mV 7.846 % 5.000 54.93 mV Worst: 18 Max 19.6 mV 7.000 764.7 mV Sum 7.98.2 kV 953.8 % 611.0 54.28 V Sum 54.28 kV 953.8 % 611.0 54.28 V Trial 18 764.681000000 mV 9.2% 7 764.680981636 f	Test Report Pass Test Configuration Details Application Name Device Description Test Description	PCIe Compliance Probe
Messages D Summaries (click for details) D 2019-01-24 11:49:58:408 AM Ready A 2019-01-24 11:49:59:025 AM Concord Mode Enabled Concord Mode Enabled 2019-01-24 11:50:04:463 AM Automation Started Concord Mode Enabled 2019-01-24 11:50:04:463 AM Automation Ended Concord Mode Enabled 2019-01-24 11:50:04:582 AM Automation Ended Concord Mode Ended 2019-01-24 11:50:04:691 AM Run Started Concord Mode Ended 2019-01-24 11:50:04:691 AM Run Started Concord Mode Ended	Device Name New Device1 Test Session Details Infinitum SW Version 11.30.00003 Infinitum Rodel Number N8900A Infinitum Serial Number 6C75353628 Debug Mode Used False Compliance Limits PCI-Express Gen5 Test Application (official) Last Test Date 2024-04-30 16:36:57 UTC -06:00	PCIe_Compliance_Probe PCIe_Compliance_Probe
Automatically invoked and	Test Statistics Margin Thresholds Failed 0 Warning < 5 %	

controlled by ADS

1.0	Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
ΙC	0	0	1	<pre>Tx, Unit interval (16.0 GT/s)</pre>	62.50000 ps	50.0000 %	62.48125 ps <= VALUE <= UpperLimit s
IΓ	0	0	1	<pre>Tx, Uncorrelated total jitter (16.0 GT/s)</pre>	1.247 ps	89.4322 %	VALUE <= TTX_UTJ_Limit s
IΓ	0	0	1	Tx, Uncorrelated deterministic jitter (16.0 GT/s)	0.00000000000 s	100.000 %	VALUE <= 6.250 ps
IΓ		0	1	Tx, Data dependent jitter (16.0 GT/s)	30 as	100.000 %	Information Only

Seasim Interface for System Designer for PCIe® (W3651B)



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ADS205

Conclusion



ADS HSD Design Flow

ADS accelerate High-Speed Digital Workflows



Conclusion

Smart Workflow for Efficient and Accurate Designs





System Designer for PCle®

A smarter design workflow for PCIe applications

Topology 3 with Retimer on Baseboard using Low-Loss PCB Material

10 inch RC to R

- · Streamlined design and simulation workflow for PCIe applications, Gen5 and Gen6 (PAM4) · Supports multi-links and multi-lanes PCIe system
- PCle_RootComplex, PCle_EndPoint, PCle_Repeater, PCle_Simulator, PCle_PreLayout, PCle_PostLayout, PCle_Tline, PCIe Probe, PCIe Compliance Probe, and PCIe Setup
- · Dedicated PCIe simulator
- · Supports Seasim Interface
- Included PCIe Compliance Tests
- · Included PCIe AMI model builder



PCle Probe (measurements: groups of signals



